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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,623	09/29/2004	Yueh-Chuan Lee	11904-US-PA-1	5622

31561 7590 02/10/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,623	LEE ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/708,227.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is a first Office action on the merits of Application Serial No. 10/711,623, which is a divisional of Application Serial No. 10/708,227 filed on 18 February 2004, now US Patent No. 6,821,842.

2. Currently, claims 1-10 are pending.

Specification

3. The specification is objected to because of the following informalities: "non-volatile" should be changed to --volatile-- after "type of" (par. 005, line 1); "106" should be changed to --104-- after "mask layer" (par. 0015, line 8); "are" should be changed to --is-- after "104" (par. 0018, line 2); "than" should be deleted after "above" (par. 18, line 6); "serves" should be changed to --serve-- after "126" (par. 0019, line 4); and "position" should be changed to --positioned-- (par. 0024, line 12). Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The meaning of the claim language "a substrate with a trench" recited in claim 1 is unclear (claim 1, line 3). Similarly, the meaning of the claim language "a substrate with a plurality of trenches" recited in claim 6 is unclear

(claim 6, line 3). There are two possible interpretations. One interpretation is "a substrate with a trench or plurality of trenches formed therein. Another interpretation is a trench or trenches formed within a layer formed on a substrate. For example, Park et al. (US 6,294,436 B1) discloses a stacked capacitor, wherein trenches 134 are formed in an insulating layer 132 formed on a substrate 102 (fig. 11). Since the claim language does not clearly specify where the trench or plurality of trenches are with respect to the substrate, that is the structural relationship between the trench or plurality of trenches and the substrate, the claim language is also open to the latter interpretation. The trench or plurality of trenches may be formed within the substrate, but the claim language does not preclude a scenario wherein the trench or plurality of trenches are within a layer formed on the substrate and not within the substrate itself. For purposes of examination, the first interpretation is being applied.

Claim Rejections - 35 USC § 102

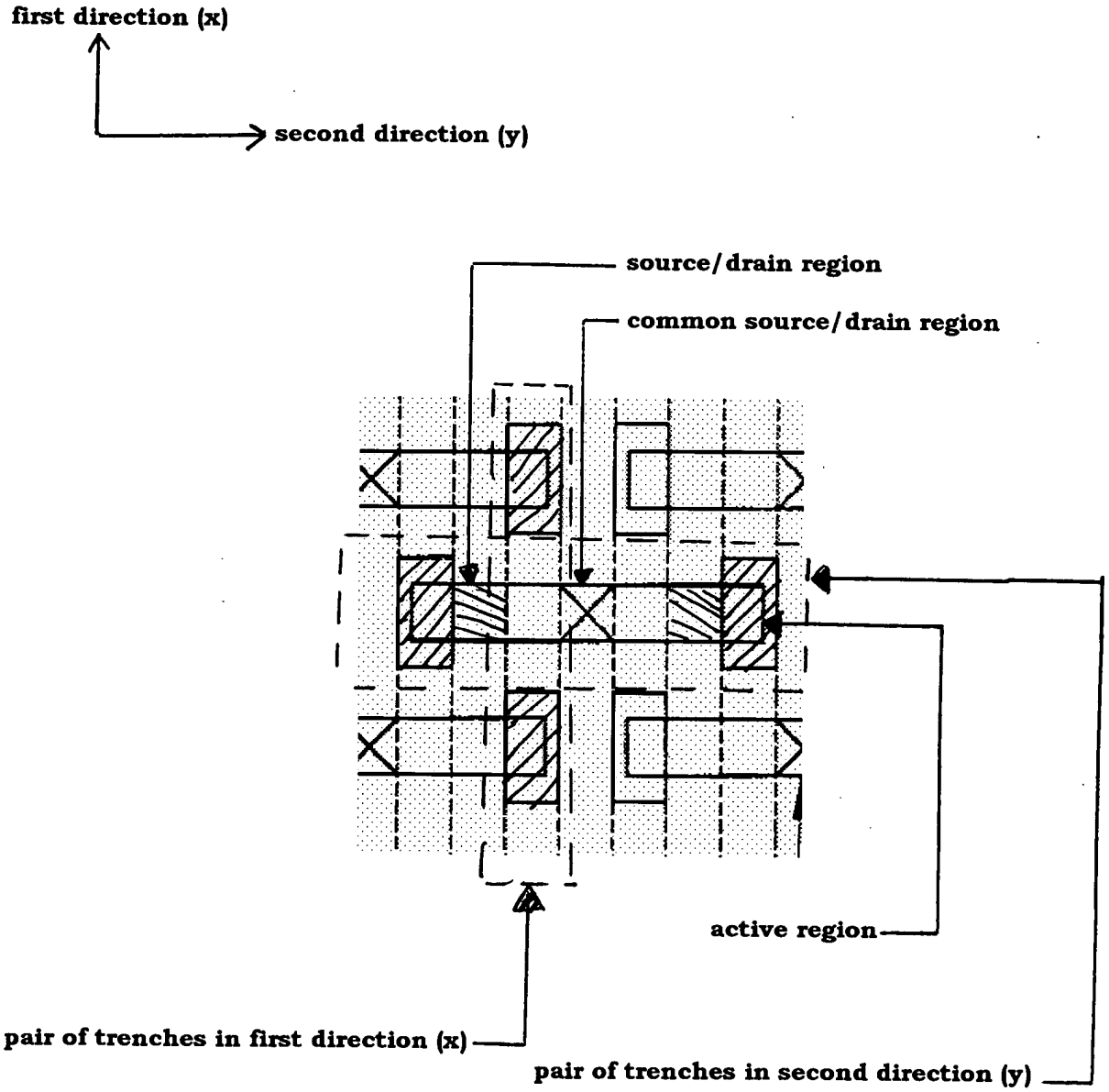
The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Hsu (US 5,994,198).

Hsu discloses a dynamic random access memory (DRAM) structure (figs. 8, 9, and accompanying text). The DRAM structure comprises: a substrate labeled silicon p-well (fig. 9) with a plurality of trenches labeled deep storage trench (fig. 8); a capacitor formed within each trench (col. 4, lines 17-22); a plurality of active regions surrounded by an isolation region, labeled STI, formed over the substrate (fig. 9); a plurality of word lines, labeled wordline conductors, running in a first direction (x) formed over the substrate (fig. 8); a plurality of source/drain regions and a plurality of common source/drain regions formed within various active regions such that a pair of source/drain region and a common source/drain region together form a group inside each active region (fig. 8); a plurality of bit lines running in a second direction (y) formed over the substrate (not shown, col. 4, lines 30-33); and a plurality of doped regions labeled p+ formed in the substrate such that dopants inside the doped region have a conductive type identical to that of the substrate (fig. 9), wherein all four side edges of each active region have a pair of trenches such that the capacitor in one of the trenches in each pair of trenches along the second direction is coupled to the active region and the capacitors in the pair of trenches along the first direction are coupled to other active regions (fig. 8), a pair of adjacent word lines passes through the active region and the two pairs of trenches along the first direction (fig. 8), and the areas in the active region

covered by the word lines serve as two channel regions; moreover, the doped regions are formed on each side of each channel region adjacent to the isolation region (fig. 9); and each source/drain region within each active region is electrically connected to a capacitor and the common source/drain region is electrically connected to a bit line (fig. 8).



Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-5 and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. in view of DeBrosse (US 5,614,431).

While Hsu discloses a DRAM structure comprising a trench storage capacitor, Hsu does not disclose the structure of the trench capacitor as recited in claims 2-5 and 7-10. DeBrosse discloses a DRAM structure, wherein the DRAM structure comprises a trench capacitor (figs. 2-9 and accompanying text). The trench capacitor comprises: an external electrode 14 in a substrate formed at a lower section of a trench 15 (fig. 2 and col. 2, lines 53-56); a capacitor dielectric layer 17 formed on the surface of the trench (fig. 2 and col. 2, lines 56-58); and a first conductive layer 18 formed inside the trench and electrically connected to a corresponding source/drain region (fig. 2 and col. 2, lines 56-58); a collar dielectric layer 19 formed on the sidewall above the first conductive layer (fig. 2 and col. 2, lines 57-60); and a second conductive layer 20 formed over the first conductive layer surrounded by the collar dielectric

layer such that the first conductive layer connects electrically with a corresponding source/drain region through the first conductive layer (fig. 2 and col. 2, lines 57-60); and a third conductive layer 21 and a buried strap 27 such that the third conductive layer is formed over the collar dielectric layer and the second conductive layer, and is electrically connected to a corresponding source/drain region through the buried strap (fig. 2 and col. 2, lines 59-61; fig. 9 and col. 3, lines 9-14). The third conductive layer 21 has a top surface below a top surface of the substrate (fig. 2).

Both Hsu and DeBrosse are from the same field of endeavor. Thus, the purpose for which DeBrosse is being relied upon would have been recognized in Hsu by one of ordinary skill in the art at the time the invention was made.

The architecture of the DRAM array described in Hsu is a folded bit line (col. 4, lines 22-27). The area of the unit cell is eight square minimum features ($8F_2$) (col. 4, lines 22-27). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form the storage trench capacitors of Hsu using the storage trench capacitors taught by Debrosse, because the trench capacitors taught by Debrosse are compatible with an $8F_2$ folded bit line DRAM array.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The

fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
04 February 2005

Mary Wilczewski
Primary Examiner